

Implementation Of Bl-Luo Converter Using FPGA

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Abstract: Luo converters are a type of dc-dc boost converters. Many power electronics applications require regulated dc supply voltage. But the available voltage is AC. Hence we require two stage power conversions. This may cause disturbances in many power quality indices such as power factor, total harmonic distortion etc. Bridgeless (BL) configurations of converters gained more importance for the past few decades. This paper presents the Matlab/Simulink modeling and the FPGA based hardware implementation of BL-Luo converter.

Keywords: Field Programmable Logic Array, Discontinuous Current Mode, Voltage Lift

I. INTRODUCTION

The necessity of better power excellence at the AC mains becomes crucial for electrical devices as enforced by International PQ standards like IEC61000-3-2. The demand of pf is greater than 0.9 and the THD is less than 5% for class D (under 600W, ≤ 16 A, single phase) applications, advocates the usage of improved power quality converters for several applications. An uncontrolled diode bridge rectifier with bulky capacitor outturns in high distortion in input side current which concludes low PF and high THD; Due to these reasons, different improved power quality ac-dc converters are employed in motor drives[2]. Two stage power factor correctors are broadly used in practice. The first and second sections are used for the power factor correction and voltage regulation respectively. The voltage regulation part can be any converter technique which depends on our need. This two stage topology is difficult and may cause higher cost and additional losses. So it is proposed to use a single stage converter for this purpose.

Field Programmable Gate Arrays (FPGAs) are one of the fastest growing parts of the digital integrated circuit market in recent times. They can be configured to implement complex hardware architectures. FPGA reconfiguration typically requires the whole chip to be reprogrammed even for the slightest circuit change.

Either Continuous conduction mode (CCM) or discontinuous conduction mode (DCM) can be used as the

IPQC designs of operation. The advantage of CCM is lesser stress on a PFC converter switches. But this mode needs two control loops for attaining PFC [3]. For this action three sensors are required, which is costly. Therefore applications having high power ratings will prefer this method. Conversely, converter working in DCM acts as an inherent power factor corrector and hence requires a single voltage control loop for dc link voltage control. However DCM is preferred for low power applications as a higher stress on the PFC converter switch is obtained in a PFC converter working in a discontinuous conduction mode.

Converter topology based on a SEPIC converter operating in DCM has been proposed for unipolar excitation of brushless dc motors [4]. The advantages are (a) the converter uses only four controlled switches, all of which are referenced to ground. This considerably simplifies their gate drive circuitry and results in low cost and compact packaging. (b) It is capable of bucking or boosting the available input dc voltage to maximize the current-regulated operation of the drive. (c) The input current naturally follows the input voltage to a certain extent, reducing the amount of low-order harmonics and resulting in a high power factor. (d) Eliminates the possibility of shoot-through faults which could occur in bipolar converters. (e) Lower conduction and switching losses because of the presence of only one switch and diode per phase as opposed to two in the bipolar case.

Bridgeless converter topologies have gained significance in the last few years due their higher efficiency. The front end

DBR is eliminated in this configuration, this results reduction in conduction losses. The PF and THD of bridgeless boost converter at full load is more improved one than the bridge type boost converter. Bridgeless PFC boost converter has larger common mode noise than conventional PFC boost converter. Limited voltage conversion ratio is the main disadvantage [5].

A new bridgeless single phase ac-dc power factor correction (PFC) rectifiers based on Buck topology operating in Discontinuous Capacitor Voltage Mode (DCVM) is proposed [6]. The DCVM operation offers additional advantages such as: zero-voltage turn-off in the power switches, zero-voltage turn-on in the output diode, and continuous input current. The electromagnetic interference (EMI) noise emission is minimized. The voltage conversion ratio is limited (<1). The output inductance is required to be large enough to maintain constant output current during one switching cycle.

In [7] operation of bridge less Luo converter is discussed.

II. LUO CONVERTER

The voltage lift (VL) technique is a widely used technique in electronic circuit design. Since the last century it has been widely applied in the design of DC-DC converters. The effect of parasitic elements limit the output voltage and power transfer efficiency of DC-Dc converters. The application of VL technique reduces these problems and improves the circuit characteristics. Luo converter is an example for converters having VL technique. Many versions of Luo converters are available. Some of them are Positive output Luo converter, Negative output Luo converter, Re-lift, Supper lift etc.

Luo converters are another series of new Dc-Dc boost converters. These converters are quite different from existing boost converters. The Advantages of Luo converters are low output voltage ripple, high power density, and cheap topology and simple structure, Smooth converter current and high efficiency.

A positive output Luo converter configuration is shown in fig.5.1. It consists of two inductors (one is the input inductor and other is the output inductor), two capacitors one diode and a switch.

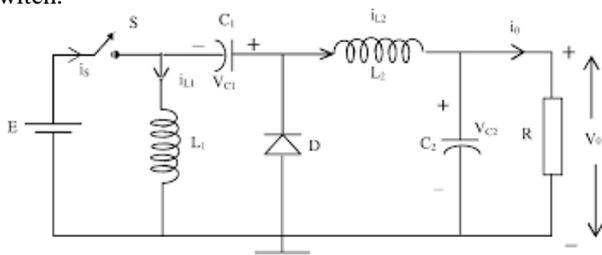


Figure 1: Positive output Luo converter

III. BL-LUO CONVERTER

The bridgeless converter topologies have gained more significance in the last few years because of their higher effectiveness than the bridged configurations. In BL configuration the conduction loss can be reduced by reducing

the number of semiconductor components in the line current path. Also BL converter has larger common mode noise and improved PF and THD. In fig.5.2, in addition to diodes D_p and D_n , which are slow recovery diodes, a second inductor is also added, resulting two dc/dc circuits, one for each half line cycle. The converter operation is divided into two parts: operation during the positive and negative half cycles of supply voltage and operation for the period of the complete switching cycle. The converter is designed to operate in Discontinuous inductor current Conduction Mode. That is the input inductor (I_{L1}, I_{L2}) currents are discontinuous in nature. The switch S_{w1} will operate at positive half cycles and S_{w2} will operate at the negative half cycles.

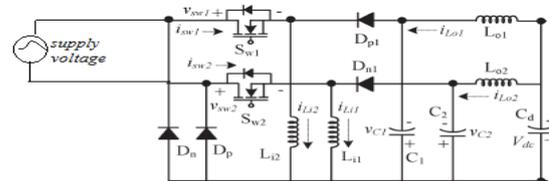


Figure 2: Circuit diagram of Bridgeless Luo converter

A. OPERATION DURING EACH HALF CYCLE OF INPUT VOLTAGE

The Bridge Less converter is designed such that two distinct switches operate for two half cycles of input supply voltage. The switch S_{w1} , inductors L_{i1} and L_{o1} , diodes Diode 1 and D_p will operate for the period of positive half cycle of the supply. The input inductor L_{i1} is designed to operate in DICM. Hence the converter have three modes of operation during the positive half cycle of supply voltage. The switching frequency of the converter is high hence several numbers of switching repetitions may occur during each half cycle. The S_{w2} , L_{i2} and L_{o2} , Diode and D_n will take part in operation for the duration of negative half cycle. In BL-Luo converter the diode bridge circuit is eliminated. The two switches and two diodes will do the same function of DBR.

B. OPERATION THROUGH COMPLETE SWITCHING CYCLE

The entire switching cycle include six modes of operation. That is each half cycle consists of three modes.

MODE I

In mode 1 S_{w1} is switched on, the inductor (L_{i1}) stores electrical energy. The amount of energy depends on the current ($i_{L_{i1}}$) passing through it and the inductance (L_{i1}). In addition to that, the energy accumulated in the capacitor (C_1) is shared to the dc-output side capacitor (C_d) and the output side inductor (L_{o1}). Thus, the voltage across the capacitor C_1 (V_{C1}) reduces, while the current in the output inductor ($i_{L_{o1}}$) and the dc- voltage (V_{dc}) are increased.

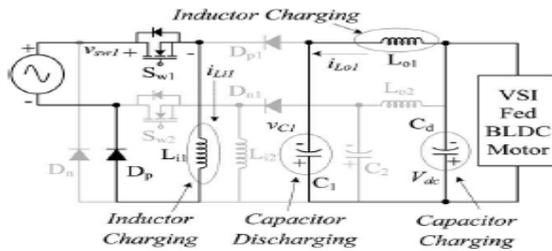


Figure 3: Mode I

MODE II

In mode 2 S_{w1} is switched off, the inductor (L_{i1}) delivers its energy to the in-between capacitor (C_1) through diode D_p . Thus, the current $i_{L_{i1}}$ reduces until it becomes zero, but the voltage across the intermediary capacitor (V_{c1}) increases. In this mode of operation the dc-side capacitor (C_d) will provide the necessary energy for the load; for this reason, the dc-link voltage V_{dc} decreases.

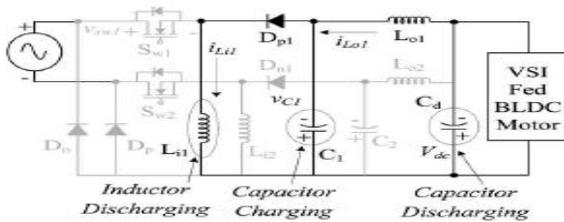


Figure 4: Mode II

MODE III

In this mode the energy remaining in the input inductor (L_{i1}), is zero. i.e., current $i_{L_{i1}}$ the inductor enters the DICM operation. During this period the in-between capacitor (C_1) and output inductor (L_{o1}) are discharged; that's why, current $i_{L_{o1}}$ and voltage V_{c1} get decreased. At the same time dc-link voltage V_{dc} increases.

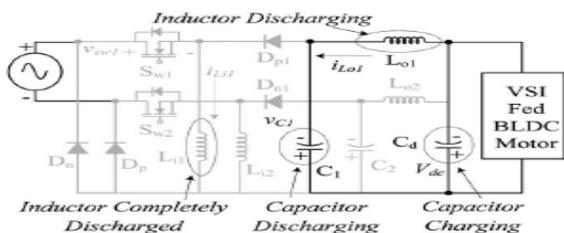


Figure 5: Mode III

These three modes of operation will repeats when switch S_{w1} is turned on again.

In a similar approach the inductors L_{i2} and L_{o2} , diode and in-between capacitor C_2 conduct to attain a required operation during the negative half cycle of the supply voltage.

IV. DESIGN

The BL-Luo converter is premeditated to work at DICM to perform as a pf pre regulator. During a switching period the inductor currents L_{i1} and L_{i2} are discontinuous in nature, where as the inductors L_{o1} and L_{o2} are continuous and the

intermediary capacitor voltages (V_{c1} and V_{c2}) remains constant.

The average input voltage at the input of the filter is given as

$$V_{in} = \frac{2\sqrt{2} \cdot V_s}{\pi} \quad (1)$$

The relation between input voltage and output voltage of the converter is

$$d = \frac{V_{dc}}{V_{dc} + V_{in}} \quad (2)$$

From the above equation the maximum and minimum duty ratios corresponding to V_{dcmax} and V_{dcmin} can be calculated. The key value of inductor L_{ic} working in DICM for duty ratio d_{min} is given as

$$L_{ic} = \frac{d_{min}(1-d_{min}) \cdot V_{in}}{2I_o f_s} \quad (3)$$

The switching frequency is f_s and the load current is I_o . The value of the intermediary capacitors (C_1 and C_2) for the duty cycle d_{max} is given as

$$C_{1,2} = \frac{d_{max} V_c}{2f_s R_L (\frac{\Delta V_c}{2})} \quad (4)$$

R_L is the load resistance, ie, $(\frac{V_{dc} + V_{dc}}{P_{max}})$, V_c is the voltage across the capacitors (C_1 and C_2) ie, $V_{dc} + V_{in}$ and ΔV_c is the allowed ripple in voltage, is taken as 60% of V_c . The value of output inductors L_{o1} and L_{o2} for the approved current ripple in the inductors is designed as follows.

$$L_{o1,2} = \frac{d_{max} I_o}{16 C_{in} f_s^2 (\frac{\Delta I_o}{2})} \quad (5)$$

The value of dc capacitor (C_d) for the duty ratio d_{min} as

$$C_d = \frac{I_o}{2w_L \Delta V_{dcmin}} \quad (6)$$

ΔV_{dc} Represents the allowed voltage ripple in the dc side capacitor (taken as 3%) and w_L is the line frequency in rps. In order to eliminate the reflection of current ripple in the supply system an input filter is needed. The maximum value of input capacitor value is given as

$$C_{max} = \frac{I_{peak}}{w_L V_{peak}} \tan(\theta) \quad (7)$$

Where V_{peak} and I_{peak} represent the peak value of the supply voltage and supply current and θ is the displacement angle between the supply voltage and current. The value of input filter inductance can be calculated from the below equation.

$$L_f = L_{req} + L_s \quad (8)$$

The cutoff frequency is f_c which is selected in such a way that $f_L < f_c < f_s$. From the above design equations the Luo converter parameter values were designed. A 400W Luo converter is designed for feeding dc voltage for the VSI fed BLDC motor. The parameter values are as follows

Parameter	Value
Input filter inductor L_s	3.77mH
Input inductors L_{i1} and L_{i2}	398μH
Output inductors L_{o1} and L_{o2}	1.78mH
Capacitors C_1 and C_2	0.419μF
Dc link Capacitor C_d	220μF
Filter capacitor C_f	330nF
Switching frequency f_{sw}	20kfz

Table 1: Circuit Parameter

V. SIMULATION RESULTS AND DISCUSSIONS

A 400W BL-Luo converter modeled using Matlab/Simulink model. The switching frequency for the converter is 20kHz. The waveforms associated with the converter is shown below. The converter is designed to operate in discontinuous mode of operation.

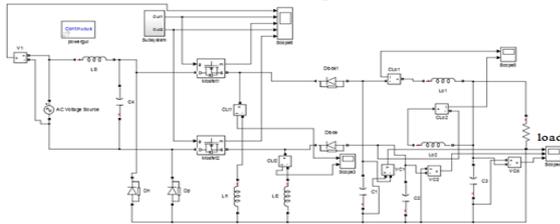


Figure 9: Simulink model of BL-Luo converter

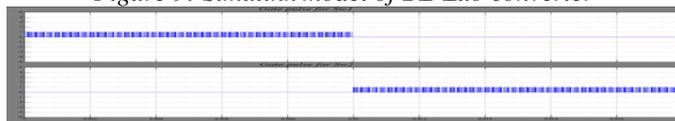


Figure 10: Gate pulses (d=50%)

X axis: time 1 div =2ms; Y axis: voltage 1 div =1V

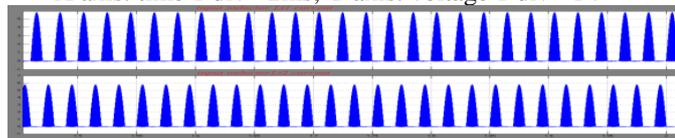


Figure 11: Input inductor currents at d=50%

X axis: time 1 div =0.05s ; Y axis: current 1 div =1A

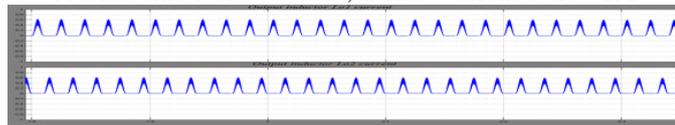


Figure 12: Output inductor currents at d=50%

X axis: time 1div =0.1s ; Y axis: current 1 div =0.2A

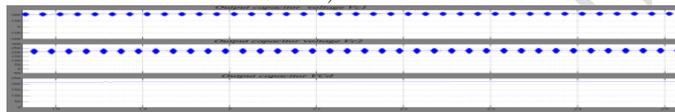


Figure 13: Output capacitor voltages at d=50%

X axis: time 1 div=0.1s; Y axis: voltage 1 div 50V

VI. HARDWARE IMPLEMENTATION

First phase for the hardware implementation is the generation of PWM pulses for BL- Luo converter using FPGA. The second phase is the design of Driver and isolation circuit using TLP-250 and third phase involves the design of Power circuit (BL-Luo converter), heat sink etc. MOSFET (IRFP450) as power switches for the Luo converter.

If the prototyping platform uses a FPGA to run the algorithm, it can be used not only to simulate exactly the hardware but also to automatically generate the VHDL code needed for the implementation. This software is the Xilinx System Generator (XSG), a toolbox working in MATLAB/SIMULINK environment.

In BL-Luo converter two MOSFET switches are there. Only one switch is operating for each half cycles of the supply voltage. Therefore two separate switching pulses are needed. The counter is used to generate a repeating sequence of 20 KHz which is compared with a constant value for generating a

20 KHz pulse. The switches Sw1 operates for the positive half cycle of the supply voltage and switch Sw2 operates for negative half cycle. In order to generate such type of pulse, initially we generated a 50 Hz pulse. Then by the logical operations we got the 20 KHz pulses for both the switches.

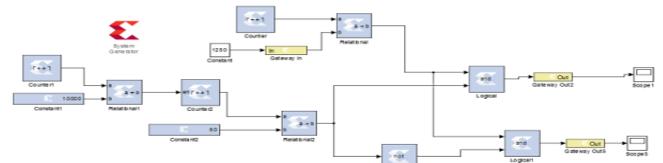


Figure 14: Xilinx Implementation for pulse generation for Luo converter

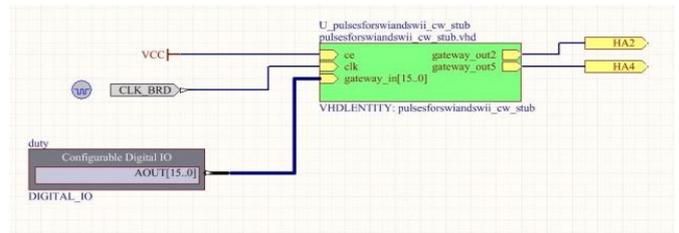


Figure 15: Circuit in ALTIUM Designer

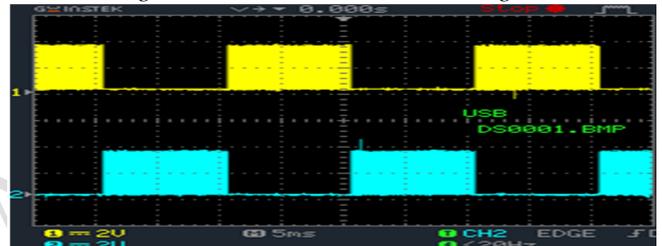


Figure 16: Pulses obtained at the output of FPGA

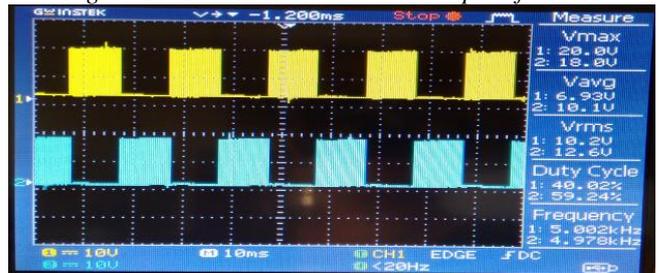


Figure 17: Pulses obtained from driver circuit (TLP 250)

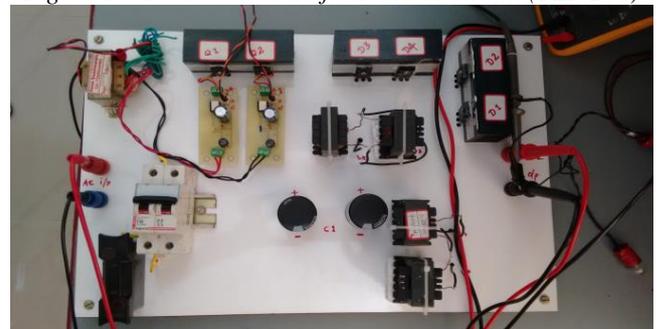


Figure 18: Hardware setup of FPGA based Luo converter

VII. CONCLUSION

In this paper, the BL-Luo converter is implanted using FPGA technique. The waveforms of output voltage and output currents are obtained. Implementation using FPGA is quite

simple. BL-Luo operating in DICM is suitable for low power applications.

REFERENCES

- [1] Limits for Harmonic Current Emissions (Equipment input current ≤ 16 A per phase), International Std. IEC61000-3-2, 2000
- [2] B. Singh, "A review of single-phase improved power quality ac dc converters," *IEEE Trans. Ind. Electron.*, vol. 50, no. 5, pp. 962–981, Oct. 2003
- [3] S. Singh and B. Singh, "A voltage-controlled PFC Cuk converter based PMBLDCM drive for air-conditioners," *IEEE Trans. Ind. Appl.*, vol. 48, no. 2, pp. 832–838, Mar./Apr. 2012
- [4] M. Mahdavi and H. Farzanehfard, "Bridgeless SEPIC PFC rectifier with reduced components and conduction losses", *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4153–4160, Sep. 2011
- [5] L. Huber, Y. Jang, and M. M Jovanovic, "Performance evaluation of bridgeless PFC boost rectifiers", *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1381–1390, May 2008
- [6] Y. Jang and M. M. Jovanovi'c, "Bridgeless high-power-factor buck converter", *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 602–611, Feb. 2011
- [7] B .Singh, "Power factor correction in bridgeless –Luo converter-fed BLDC motor drive," *IEEE Trans. Ind. Appl.*, vol. 51, no.2, pp. 1179-1188, Mar./Apr. 2015
- [8] Sumanth Donthi, and Roger L. Haggard, "A survey of Dynamically reconfigurable FPGA devices," Proceedings of the 35th South eastern Symposium on System Theory, pp. 422 –426, 2003.

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